REMARKS

Applicants respectfully request consideration of the subject application as amended herein. This Amendment is submitted in response to the Office Action mailed November 29, 2005. Claims 24-34 have been withdrawn. Claims 1-23 are rejected. In this Amendment, Claims 12-13 has been amended. No claims have been canceled. Claims 35-37 has been added. Applicant submits that no new matter is added.

Amendment to the Drawings

The Examiner has objected to the drawings. Applicant has amended the drawings to include the Legend that reads "Prior Art" in Figures 1-2.

Applicant has also amended Figure 4 and 5 to indicate that $Z=Z_1+ Z_2+ Z_3$ as discussed in the Specification. Applicant submits that no new matter is added by the amendment of the drawings.

Rejections under 35 U.S.C. § 102(b)

The Examiner has rejected claims 12-14 and 18-23 under 35 U.S.C. §102(b) as being anticipated by Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design" ("Ito-Design"). Applicant respectfully submits that for at least the reasons discussed below, the pending claims are patentable over Ito-Design. Claim 12 in its currently amended form recites,

> 12. (Currently Amended) A method of creating tensile stress in a silicon substrate comprising:
> providing a substrate;

creating a shallow trench isolation (STI) region between sections of the substrate;

forming a source region and a drain region in the substrate for a semiconductor device, wherein at least two section selected from the plurality of sections of the substrate form one source region and at least two section selected from the plurality of sections of the substrate form one drain region; and

forming a tensile inducing layer over the substrate, the tensile inducing layer being an insulation material capable of causing tensile stress in the substrate.

Applicant's claimed invention taught a novel method of enhancing a strained semiconductor device that is not taught in Ito-Design. Ito taught that a silicon nitride layer is formed directly over a transistor to increase stress in the p-n junction. Ito-Design further evaluated different types of nitride layers. Ito-Design, however, did not teach that multiple narrow sections are used to form one single source section and similarly, did not teach that multiple narrow sections are used to form one single drain sections as recited in Applicant's claimed invention. Merely based on a knowledge that multiple STI regions can be formed in a substrate used to isolate multiple transistor devices cannot be taken to say that multiple STI regions are formed into ONE source/drain region to form a multi-narrow-lane source/drain region. In other words, conventional source/drain regions are continuous whereas Applicant's invention taught a source/drain regions that each has multiple lanes forming one region.

In contrast to Ito-Design, Applicant's claim 12 clearly recites that "...a shallow trench isolation (STI) region between sections of the substrate;" and "forming a source region and a drain region in the substrate for a semiconductor device, wherein at least two section selected from the plurality of sections of the substrate form one source region and at least two section selected from the plurality of sections of the substrate form one drain region;" and "forming a

tensile inducing layer over the substrate." These features are completely lacking from Ito-Design.

With respect to the Examiner's point to Table 1 and pages 247-248 of Ito-Design to teach Applicant's claimed invention, Applicant respectfully disagrees. Ito-Design's Table 1 merely lists the physical properties of the nitride films used in the Experiment of forming the nitride film over the transistor. As for the remainder, Ito-Design did not teach or even use a multiple-narrow-section source region or drain region as a way to enhance a strained semiconductor device with a nitride layer. Again, Ito merely taught that a nitride layer is used to deposit over the transistor to effect a mechanical stress in the junction. But Applicant's invention went further than that; Applicant's invention enhances multiple directions by making each source/drain section a multi-narrow lanes section. Therefore, at least for the reasons above, Applicant respectfully submits that Ito-Design did not anticipate claim 12.

Claims 13-14 and 18-23 depend indirectly or directly from claim 12 and are thus similarly not anticipated by Ito-Design for the same reasons.

The Examiner has also rejected claims 12-14 and 18-23 under 35 U.S.C. §102(b) as being anticipated by Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement" ("Shimizu"). Applicant respectfully submits that for at least the reasons discussed below, the pending claims are patentable over Shimizu.

Shimizu is similar to Ito-Design and likewise, lacked the teaching of multiple narrow sections are used to form one single source section and similarly, did not teach that multiple

narrow sections are used to form one single drain sections as recited in Applicant's claimed invention.

Shimizu taught simply that a silicon nitride layer is formed over a transistor or two to increase stress in the p-n junction. Shimizu taught also that the nitride layer affects the strain in the channel of a MOSFET. But, similar to Ito-Design, Shimizu did not teach that multiple narrow sections are used to form one single section such as a source section or a drain section as recited in Applicant's claimed invention. Merely based on the teaching that that nitride layer is formed to increase stress in the channel does not in any way teach that STI regions can be formed into ONE source/drain region to form a multi-narrow-lane source/drain region. In the prior art, a source and drain region are continuous regions and not formed with multiple lanes.

In contrast to Shimizu, Applicant's claim 12 clearly recites that "...a shallow trench isolation (STI) region between sections of the substrate;" and "forming a source region and a drain region in the substrate for a semiconductor device, wherein at least two section selected from the plurality of sections of the substrate form one source region and at least two section selected from the plurality of sections of the substrate form one drain region;" and "forming a tensile inducing layer over the substrate." These features are completely lacking from Shimizu. Therefore, at least for the reasons above, Applicant respectfully submits that Shimizu did not anticipate claim 12.

Claims 13-14 and 18-23 depend indirectly or directly from claim 12 and are thus similarly not anticipated by Shimizu for the same reasons.

The Examiner has also rejected claims 1-23 under 35 U.S.C. §102(b) as being anticipated by Ito, et al., "Effect of Mechanical Stress Induced by Etch-Stop Nitride: Impact

on Deep Submicron Transistor Performance" ("Ito-Performance"). Applicant respectfully submits that for at least the reasons discussed below, the pending claims are patentable over Ito-Performance.

Ito-Performance lacked the same elements of claims 1-23 as previously discussed with respect to Ito-Design and Shimizu. Particularly, Ito-Performance did not teach that multiple narrow sections are used to form one single source section and similarly, did not teach that multiple narrow sections are used to form one single drain sections as recited in Applicant's claimed invention. Simply that that multiple STI regions can be formed in a substrate used to isolate a device and used to isolate multiple transistor devices from one another is not the same as one region of a device has multiple narrow lanes such as ONE source/drain region having a form a multi-narrow-lane source/drain region. For example, as recited in claim 1, "creating a shallow trench isolation (STI) region between each two sections of the source region and between sections of the drain region" where "each of the source region and the drain region includes a plurality of sections..." are not the same as a semiconductor device having a trench isolation, a gate stack, and source and drain regions as a conventional device.

Therefore, at least for the reasons above, Applicant respectfully submits that Ito-Performance did not anticipate claims 1-23.

Rejections under 35 U.S.C. § 102(e)

The Examiner has rejected claims 12-14, and 18-20 under 35 U.S.C. §102(e) as being anticipated by Toda, (U.S. Patent Application 2005/0032275, hereinafter "Toda"). As discussed below, the pending claims are patentable over the above reference. Applicant respectfully submits that for at least the reasons discussed below, the pending claims are

patentable over Toda.

Toda lacked the same elements of claims 1-23 as previously discussed with respect to Ito-Design, Ito-Performance, and Shimizu. Particularly, Toda did not teach that multiple narrow sections are used to form one single source section and similarly, did not teach that multiple narrow sections are used to form one single drain sections as recited in Applicant's claimed invention. Simply that that multiple STI regions can be formed in a substrate to isolate a device and used to isolate multiple transistor devices from one another is not the same as one region of a device has multiple narrow lanes such as ONE source/drain region having a form a multi-narrow-lane source/drain region. For example, as recited in claim 1, "creating a shallow trench isolation (STI) region between each two sections of the source region and between sections of the drain region" where "each of the source region and the drain region includes a plurality of sections..." are not the same as a semiconductor device having a trench isolation, a gate stack, and source and drain regions as a conventional device.

Therefore, at least for the reasons above, Applicant respectfully submits that Toda did not anticipate claims 12-14, and 18-20.

The Examiner has also rejected claims 1-8, 11-20 and 23 under 35 U.S.C. §102(e) as being anticipated by Yeo, (U.S. Patent Application 2004/0212035, hereinafter "Yeo").

Yeo lacked the same elements of claims 1-8, 11-20 and 23 as previously discussed with respect to Ito-Design, Ito-Performance, Shimizu, and Toda. Particularly, Yeo did not teach that multiple narrow sections are used to form one single source section and similarly, did not teach that multiple narrow sections are used to form one single drain sections as recited in Applicant's claimed invention. Simply that that multiple STI regions can be formed in a substrate to isolate a device and used to isolate multiple transistor devices from

one another is not the same as one region of a device has multiple narrow lanes such as ONE source/drain region having a form a multi-narrow-lane source/drain region. For example, as recited in claim 1, "creating a shallow trench isolation (STI) region between each two sections of the source region and between sections of the drain region" where "each of the source region and the drain region includes a plurality of sections..." are not the same as a semiconductor device having a trench isolation, a gate stack, and source and drain regions as a conventional device.

It can be seen from the Examiner's understanding of Figure 6b, for example, that Yeo used trench isolation 220 for isolate devices 236 and device 238. Within each of those devices, there are source and drain regions 250 and 254, for example. Yeo lacked the teaching that each of those source and drain regions can be made to include multiple narrow lanes separated by STI regions recessed into the surface as claimed by Applicant's invention.

Therefore, at least for the reasons above, Applicant respectfully submits that Yeo did not anticipate claims 1-8, 11-20 and 23.

Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected claims 1-11 and 15-17 under 35 U.S.C. §103(a) as being unpatentable over Ito or Shimizu and Applicant's admitted prior art. Applicant submits that at least for the reasons above, claims 1-11 and 15-17 are also not made obvious over Ito or Shimizu in view of Applicant's admitted prior art.

Newly added claims 35-37

Applicant submits that the newly added claims contain similar subject matter as the pending claims and that the cited art, Ito, Shimizu, Toda, and Yeo did not teach claims 35-37 for at least the same reasons stated above.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Mimi Dao at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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